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An Improved Bridgeless SEPIC PFC Converter

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Abstract—In power electronic converters, active power factor correction circuits (PFC) are employed to correct the power factor and achieve high efficiency. Single-ended primary inductor converter (SEPIC) can provide a high power factor. This conventional power factor correction SEPIC suffers from high conduction loss at the input bridge diode. To overcome this problem, a bridgeless SEPIC converter with ripple-free input current is proposed. In the proposed bridgeless converter, the input bridge diode is removed and the conduction loss is reduced. The input current ripple is reduced by means of an auxiliary circuit. The auxiliary circuit consists of an additional winding of the input conductor, an auxiliary small inductor and a capacitor. In this converter, the input current in a switching period is proportional to the input voltage and near unity power factor is achieved. Thus the proposed converter has the advantages of both reduction of ripple current and conduction losses which increases the efficiency of the converter and it is also capable of efficient power factor correction. The operating principles and the waveforms of the converter are analyzed and the performance of the proposed converter is verified by MATLAB simulations.

Index Terms—Bridgeless converter, coupled inductor, power factor Correction (PFC), single-ended primary inductor converter (SEPIC).

1 INTRODUCTION

According to the demand on high efficiency and low Harmonic pollution , the active power factor correction (PFC) circuits are commonly employed in ac–dc converters and Switched - mode power supplies. Generally, these kinds of converters include a full-bridge diode rectifier on an input current path so that conduction losses on the full-bridge diode occur and it will be worse especially at the low line. To overcome this problem, bridgeless converters have recently been introduced to reduce or eliminate the full-bridge rectifier, and hence their conduction losses [1]-[8].

A bridgeless boost converter is widely used in advantages of reduced input current ripple, but its output voltage should be higher than the peak voltage of the inge [6]-[10].

Since the input current of the PFC buck converter has dead angles during the time intervals when the input voltage is lower than the output voltage, there is a strong trade-off between power factor and output voltage selection. On the other hand, a SEPIC PFC converter can provide a high power factor regardless its output voltage due to its step up/down function [1]-[3]. The efficiency of these converters is improved by removing the input bridge diode. However, bulk input inductor or another LC filter is required to suppress the input current ripple.

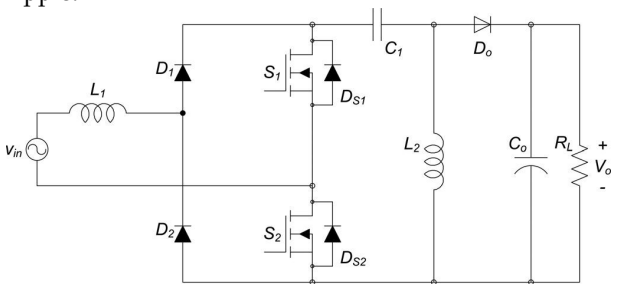


Fig.1Bridgeless SEPIC PFC Converter

In Fig. 1, a bridgeless SEPIC PFC converter is shown. The component count is reduced and it shows high efficiency due to the absence of the full-bridge diode. However, in this converter, an input inductor with large inductance should be used in order to reduce the input current ripple. In addition, the conduction losses on intrinsic body diodes of the switches are caused by using single pulse width modulation (PWM) gate signal.

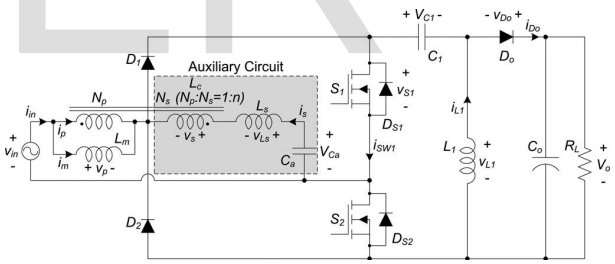


Fig.2 Proposed Bridgeless SEPIC Converter

In order to overcome these problems, a bridgeless SEPIC converter with ripple-free input current is proposed in Fig. 2.

An auxiliary circuit, which consists of an additional winding of the input inductor, an auxiliary small inductor, and a capacitor, is utilized to reduce the input current ripple. The shaded area in Fig. 2 represents the auxiliary circuit for achieving the input current ripple cancellation.

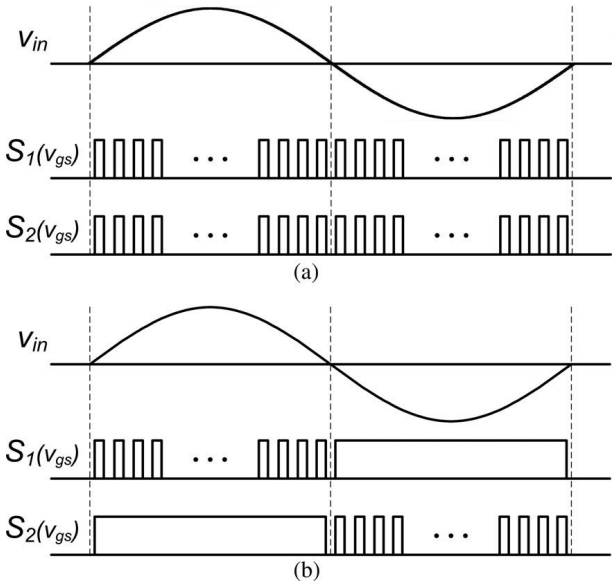


Fig. 3(b) shows the proposed gate signals for the switches.

For a half period of the input voltage, one switch is continuously turned ON and the current via an intrinsic body diode is forced to flow through the channel of the switch. It can reduce the conduction loss on the switch further and the efficiency can be improved.

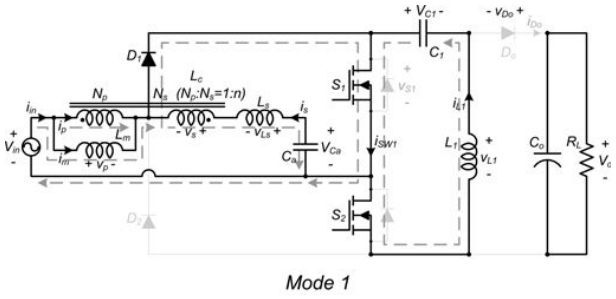
II. ANALYSIS OF THE PROPOSED CONVERTER

The auxiliary circuit includes an additional winding Ns of the input inductor Lc , an auxiliary inductor Ls , and a capacitor Ca . The coupled inductor Lc is modeled as a magnetizing inductance Lm and an ideal transformer which has a turn ratio of 1:n (n=Ns /Np).The capacitance of Ca is large enough, so Ca can be considered as a voltage source VCa during a switching period. Similarly, the average capacitor voltage VC1 is equal to Vin . Diodes D1 and D2 are the input rectifiers and operate like a conventional SEPIC PFC converter. DS1 and DS2 are the intrinsic body diodes of the switches S1 and S2 . The switches S1 and S2 are operated with the proposed gate signals shown in Fig. 3(b).

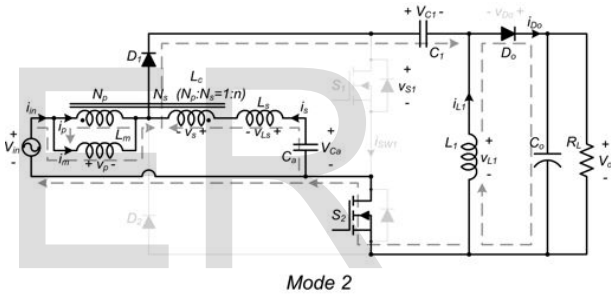
The operation of the proposed converter is symmetrical in two half-line cycles of input voltage. Therefore, the converter operation is analyzed during one switching period in the positive half-line cycle of the input voltage. It is assumed that the converter operates in discontinuous conduction mode (DCM), so the output diode Do is turned OFF before the main switch is turned ON.

The capacitance of the output capacitor *Co* is assumed sufficiently large enough to consider the output voltage *Vo* as constant. Also, the input voltage is assumed constant and equal to *V*in in a switching period T_s . The operation of the proposed converter in one switching period *Ts* can be divided into three modes. Before *t*0 , the switch S1 and the diode *Do* are turned OFF and the switch S2 is conducting. The input current is the sum of the freewheeling currents I_{s2} and I_{L2} .

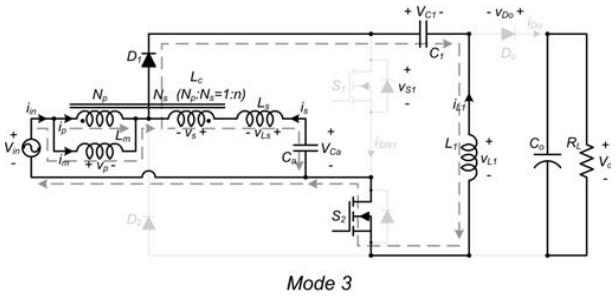
MODES OF OPERATION:



Mode 1 [t0, t1]: At *t*0 , the switch S1 is turned ON and the switch S2 is still conducting. Since the voltage V_p across L_m is V_{in} , the magnetizing current i_m increases from its minimum value I_{m2} linearly with a slope of V_{in}/L_m. The voltage V_{Ls} across L_s is equal to $(1-n)V_{\text{in}}$. Therefore, the current *is* increases from its minimum value $-I_s2$ linearly with a slope of $(1-n)V_{\text{in}}/L_s$.



Mode 2 [t1, t2]: At *t*1 , the switch S1 is turned OFF and the switch S2 is still conducting. Since the voltage V_p across L_m is $-V_o$, the magnetizing current *im* decreases from its maximum value I_{m1} linearly with a slope of $-V_o/L_m$. The voltage V_{Ls} across L_s is $-(1-n)V_o$, so that the current *is* decreases from its maximum value I_{s1} linearly with a slope of $-(1-n)V_o/L_s$



Mode 3 [t2, t'0]:

At t_2 , the current i_{Do} becomes zero, and the diode *Do* is turned OFF. In this mode, the input current *i*in is the sum of freewheeling currents I_{s2} and I_{L2} .

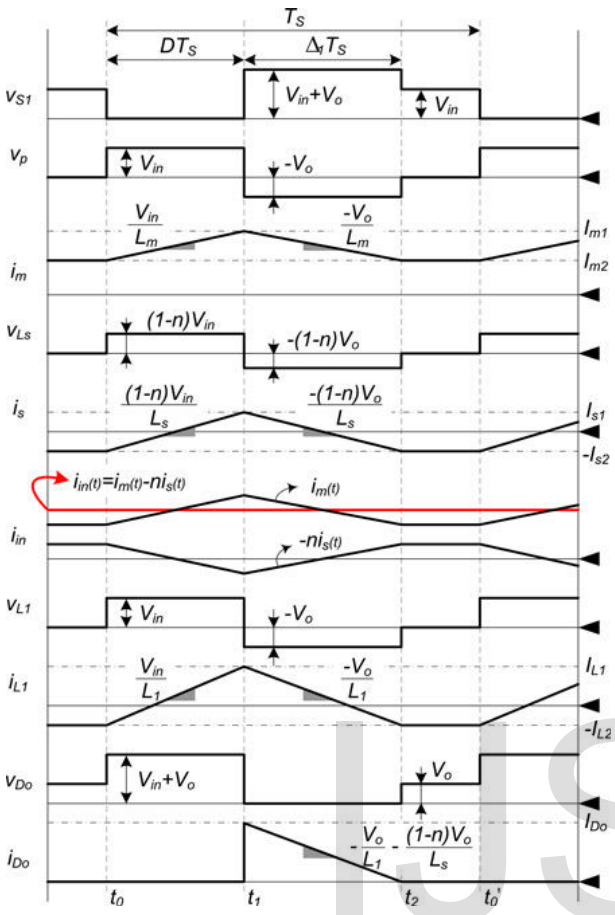


Fig.4 Key waveforms of the proposed converter.

DESIGN VALUES:

V_{in} =130 Vac, f_L =60 Hz, f_{sw} = 100 kHz, D = 0.25, Lm = 600 μH, n = 0.7, Ls = 127 μH, $L1$= 63 μH, Ca = 0.3 μF, $C1$ = 0.4 μ F, Co = 880 μF, and R_L =77 Ω.

SIMULATION DIAGRAM AND RESULTS:

CONVENTIONAL BRIDGELESS SEPIC PFC:

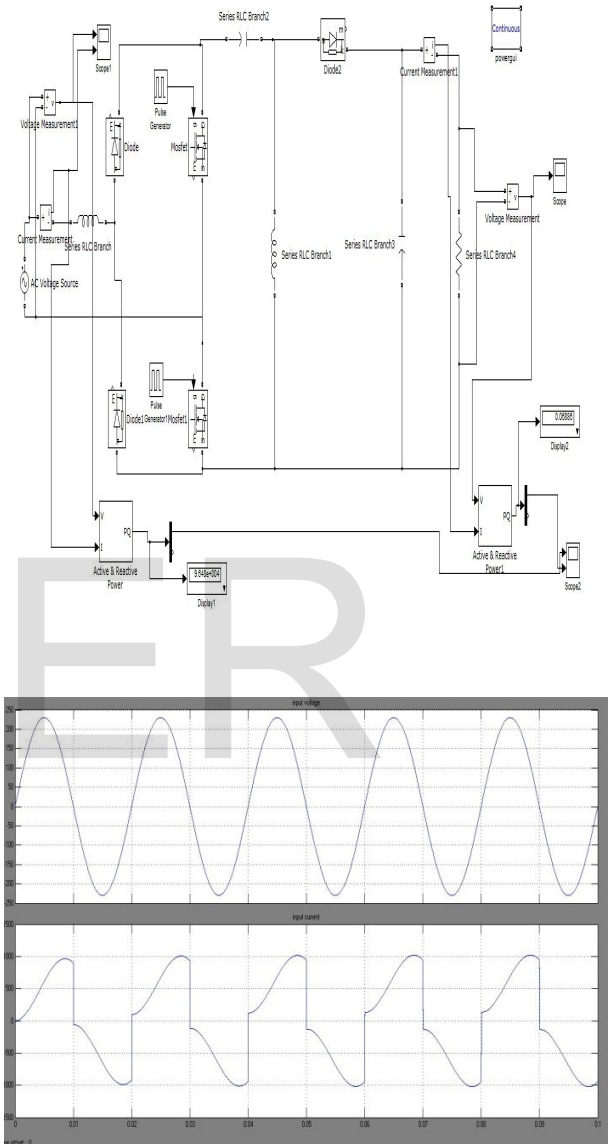


Fig.5 Input current and Input voltage of conventional Sepic PFC converter

PROPOSED BRIDGELESS SEPIC PFC:

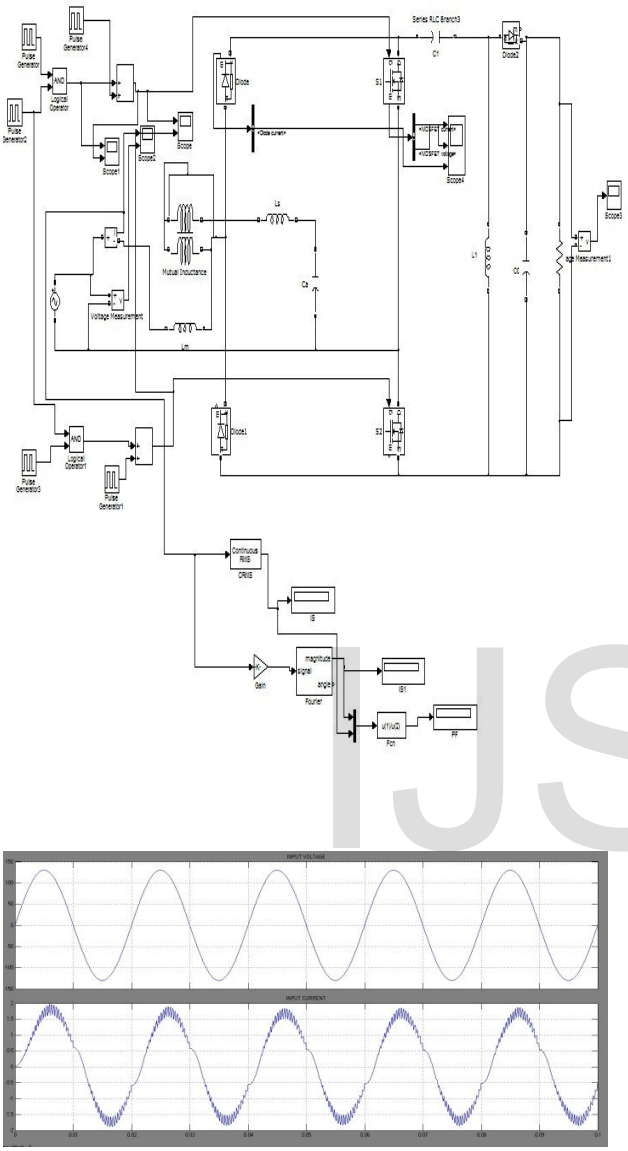


Fig.6 Input current and Input voltage

In the conventional Sepic converter it is found that the input current contains a lot of ripples and is not a replica of the input voltage. The THD is found to be 34.44%.

In the proposed Sepic converter the input current is proportional to the input voltage. The THD is nearly reduced by 50% and is found to be 8.49%. The input current is ripple free and hence the power factor is improved. A power factor of 0.99 is obtained. An output voltage of 100 V is got.

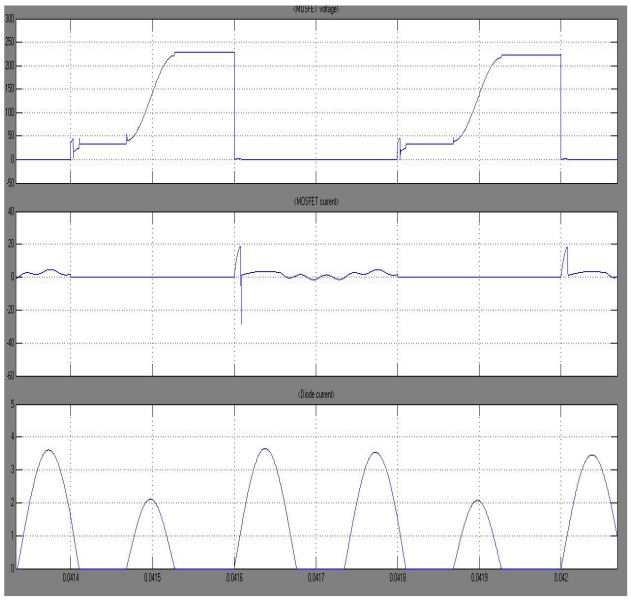


Fig.7 Waveforms of MOSFET voltage, current and diode current

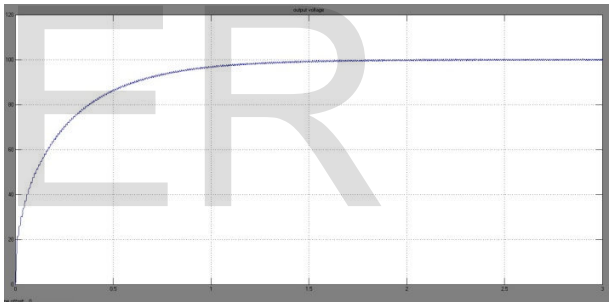


Fig.8 Waveform of output voltage

CONCLUSION:

The input current ripple is reduced by means of an auxiliary circuit. The input current is proportional to the input voltage and power factor is improved. A power factor of 0.99 is obtained. The THD of the converter is reduced and an output voltage of 100 V is obtained and thus the efficiency of the converter is improved.

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